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EXAMINER	
NGUYEN, LINH V	
ART UNIT	**PAPER NUMBER**
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/763,561	Applicant(s) MENKUS ET AL.	
	Examiner Linh V. Nguyen	Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 – 3, 8 – 12, and 14 – 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *6,7 and 28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to amendment filed on 7/26/06. Claims 1, 2, 3, 8, 11, 12, 14, 15, 16, 17, 18 and 20 have been amended. Claims 4, 5, 13 have been canceled. Claims 21 - 28 have been added. Claims 1 – 3, 6 – 12, and 14 – 28 are pending on this application.

Response to Arguments

2. Applicant's arguments to the amended and new claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

3. Claims 6 and 7 are objected to because claim 6 depended on claim 5, but claim 5 have been canceled. According claims 6 and 7 not been further treated on the merits.

Claim 28 is object to because "first bus" on line 23 of the claim needs to change to "second bus" for consistency of second output of the first amplifier circuit coupled to second bus.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1 – 3, 8 – 12, and 14 – 28 are rejected under 35 U.S.C. 102(a) as being anticipated by Galambos et al. U.S. patent No. 6,570,522.

Regarding claim 1, Fig. 2 of Galambos et al. discloses a circuit for reducing the current density on a bus (input bus lines of 26, 28, 30) coupled to a plurality of circuits (26, 28, 30), the circuit comprising: a folding (col. 1 line 49) amplifier array (24A, 24C, 24E, 24G, 24B, 24F) for a fine channel circuit (Col. 1 line 61 discloses Least Significant Bit) of a folding analog-to-digital converter (Fig. 2), wherein the folding amplifier array (24A, 24C, 24E, 24G) includes: a first amplifier circuit (first transistor of 24A) of the plurality of circuits, wherein the first amplifier circuit is configured to provide a first output current for the bus (output current of first transistor 24A); and a first current source circuit (voltage VCC and Resistor 25E provide a current (VCC/25E = I)) that arranged to provide a first local current (VCC/25E = I) at an output first amplifier circuit (current output of 24A) such that at least a portion of the first output current is prevented from being carried on the bush (current at the bus line is decreased at the node by the current of VCC/25E); a second amplifier circuit (first transistor of 24C) of the plurality of circuits, wherein the second amplifier circuit is configured to provide a second output current for the bus (output current of first transistor 24C); and a second current source circuit (voltage VCC and Resistor 25E provide a current (VCC/25F = I)) that is configured to provide a second local current (VCC/25F = I) at an output of the second amplifier circuit (output current of 24C) such that at least a portion of the second output

current is prevented from being carried on the bus(current at the bus line is decreased at the node by the current of VCC/25F).

Regarding claim 2, wherein the folding amplifier array further includes: a load circuit that is coupled to the bus (26).

Regarding claim 3, wherein the first amplifier circuit (24A) is configured to provide the first output current to the bus in response to a first input voltage signal (22A), and wherein the first output current is a differential current (differential amplifier 24A), and the first input voltage signal (22A) is a differential voltage signal (1).

Regarding claim 8, wherein the folding amplifier array further includes: another bus (second input bus line of 26) that is coupled to another plurality of circuits (24B, 24F); another amplifier circuit (24F, 24B) of the other plurality of circuits, wherein the other amplifier circuit is configured to provide another output current for the other bus (output currents of 24F, 24B); and another current source circuit (VCC/25C=I) that is arranged to provide another local current at an output of the other amplifier circuit (24B, 24F) such that at least a portion of the other output current is prevented from being carried on the other bus (the current of the bus line is decreased at the node by VCC/25C).

Regarding claim 9, (Original) The circuit of Claim 1, wherein the first amplifier (24A) circuit includes: a first differential pair (transistors pair); and a first tail current source (10) that is configured to provide a first tail current, and wherein the first local current corresponds to a fraction of the first tail current (since VCC/25E is part of the tailed current 10, VCC/25E must be a fraction of the tail current 10).

Regarding claim 10, wherein the fraction of the first tail current is approximately half of the first tail current (since tail current 10 is the sum of all currents at the node; thereby the fraction current must be approximate ½ of the tail current).

Regarding claim 11, Fig. 2 of Galambos et al. discloses circuit, comprising: an amplifier array circuit (24A to 24G) with a plurality of buses (input bus lines of 26, 28, 30) for a folding analog-to-digital converter circuit (26, 28, 30), wherein the amplifier array circuit (24A to 24G) is a folding amplifier array circuit for a fine channel stage (D0) of the folding analog-to-digital converter (Col. 1 line 61 discloses Least Significant Bit), the amplifier array circuit comprising: a plurality of transconductance circuits circuit (24A to 24G); a plurality of load circuits (26, 28, 30), wherein each of the plurality of load circuits (26, 28, 30), is separately coupled to one of the plurality of buses (input bus lines), wherein a first bus (bus line of 26) of the plurality of buses is coupled to a portion of the plurality of transconductance circuits (24A, 24C, 24E, 24G); and a first current source circuit (Vcc/25E), wherein the first current source circuit is coupled to an output of a first of the portion (24A) of the plurality of transconductance circuits, and wherein the first current source circuit (VCC/25E=I) is arranged to provide a first local current at the output of the first transconductance circuit (24A) such that a maximum magnitude of current density is decreased (current at the bus line is decreased at the node by the current of VCC/25E) on at least the first bus (first bus line of input 26) of the plurality of buses; and another current source circuit (VCC/25D) that is coupled to an output of another transconductance circuit (24B) in the portion of transconductance circuits.

Regarding claim 12, wherein one of the portion of the transconductance circuits is not saturated (24A), and wherein every other transconductance circuit (24C, 24E, 24G) in the portion is saturated.

Regarding claim 14, Fig. 2 further comprising: a plurality of current source circuits (VCC/ 2aA to VCC/25F) that includes the first current source circuit (VCC/25F), wherein each of the plurality of transconductance circuits (24A, 24B) has an output coupled to a separate one of the plurality of current source circuits (VCC/25C to VCC/25D).

Regarding claim 15, Fig. 2 of Galambos et al. discloses amplifier array circuit (24A to 24G) with a plurality of buses (input bus lines of 26, 28) for a folding analog-to-digital converter circuit (26, 28, 30), the amplifier array circuit comprising a plurality of transconductance circuits (24A to 24G); a plurality of load circuits (26, 28), wherein each of the plurality of load circuits is separately couple to one of the plurality of buses (input bus lines), wherein a first bus of the plurality of buses (first input bus line of 26) is coupled to a portion (24A) of the plurality of transconductance circuits (24A to 24 G); a first current source circuit (VCC/25E=I), wherein the first current source circuit (VCC/25E) is coupled to an output of a first of the portion (24A) of the plurality of transconductance circuits, and wherein the first current source circuit (VCC/25E) is arranged to provide a first local current (VCC/25E=I) at the output of the first transconductance circuit (24A) such that a maximum magnitude of current density is decreased on at least the first bus of the plurality of buses (current at the bus line is decreased at the node by the current of VCC/25F); and a plurality of current source

circuits (VCC/25A to VCC/25F) that includes the first current source circuit (VCC/25E), wherein each of the plurality of transconductance circuits (24A to 24G) has an output coupled to a separate one of the plurality of current source circuits (Vcc/25A to VCC/25F) wherein each of the plurality of load circuits (26, 28) includes a load current source (34, 32), and wherein each of the plurality of current source circuits (VCC/25E, VCC/25C) shares a bias line in common with one of the load current sources (see Fig. 2).

Regarding claim 16, wherein each of the plurality of transconductance circuits (24A to 24 G) is configured to provide a separate transconductance current (output currents of 24A to 24G) on one of the plurality of buses (input bus lines of 26, 28), and wherein each of the plurality of current source circuits (VCC/25A to VCC/25F) is configured to supply a separate local current (VCC/25=I) such that at least a portion of the output current from each of the plurality of transconductance circuits is prevented from being carried on each of the plurality of buses (current at the bus line is decreased at the node by the current of VCC/25).

Regarding claim 17, wherein the first transconductance circuit (24A) is configured to provide the first transconductance current (output current of 24A) in response to a differential voltage (22A; the first transconductance current is differentia (differential amplifier 24A)l; and wherein the first local current (VCC/25E) is differential.

Regarding claim 18, wherein the first transconductance circuit (24A) includes: a first differential pair (differential pair transistor of 24A); and a first tail current source (10) that is configured to provide a first tail current (10), and wherein the first local current

corresponds to a portion of the first tail current (VCC/25E is a current, which is a part of the tail current 10).

Regarding claim 19, wherein the portion of the first tail current is approximately half of the first tail current (since tail current 10 is the sum of all currents at the node; thereby the portion current must be approximate ½ of the tail current).

Regarding claim 20, Galambos et al. as applied to claim 1 above, disclosed every aspect of applicant claimed invention.

Regarding claim 21, Galambos et al. as applied to claim 1 above disclosed every aspect of applicant's claimed invention.

Regarding claim 22, wherein the bus (input bus lines is composed of metal having substantially no resistance (no resistance on the bus line in fig. 2).

Regarding claim 23, Fig. 2 of Galambos et al. discloses a circuit for reducing the current density on a bus (input bus lines of 28, 26) coupled to a plurality of circuits (24A to (24G), the circuit comprising: a first amplifier circuit (24A) of the plurality of circuits, wherein the first amplifier circuit (24A) is configured to provide a first output current (current output of 24A) for the bus; a first current source circuit (VCC/25E=I) that is arranged to provide a first local current at an output of the first amplifier circuit (24A) such that at least a portion of the first output current is prevented from being carried on the bus (output current of amplifier circuits is branched out at the node prior to 26 due to current source circuit VCC/25); and a load circuit (26, 28) that is coupled to the bus, wherein the load circuit is configured to provide an output voltage (D0) such that the

output voltage is substantially equal to the multiplicative product (24A, 24C, 24E, 24G) of the bus current, and an impedance of the load circuit (28).

Regarding claim 24, Fig. 2 of Galambos et al. discloses a circuit (VCC/25) for reducing the current density on a bus (input bus line of 26, 28) coupled to a plurality of circuits (24A to 24F), the circuit comprising: a first amplifier circuit (24A) of the plurality of circuits, wherein the first amplifier circuit (24A) is configured to a first amplifier (24A) carried on the a load impedances (26) provide a first output current (output current 24A) for the bus; a first current source circuit that (VCC/25E) is arranged to provide a first local current (VCC/25E=I) at an output of the circuit (2VCC/25E)) such that at least a portion of the first output current (output current of 24A) is prevented from being bus; and load circuit (26) that is coupled to the bus, wherein the load circuit does not include averaging impedances (26 does not discloses average impedance).

Regarding claim 25, Fig. 2 of Galambos et al. discloses a circuit (VCC/25) for reducing the current density on a bus (input bus lines of 26, 28) coupled to a plurality of circuits (24A to 24F), the circuit comprising: a first amplifier circuit (24A) of the plurality of circuits, wherein the first amplifier circuit (24A) is configured to provide a first output current (output current of 24A) for the bus; a first current source circuit (VCC/25E) that is arranged to provide a first local current (VCC/25E= I) at an output of the first amplifier circuit (24A) such that at least a portion of the first output current (output current of 24A) is prevented from being carried on the bus; and a load circuit (26) that is coupled to the bus, wherein the load circuit is coupled to a supply voltage (Voltage supply is inherent to 26).

Regarding claim 26, Fig. 2 of Galambos et al. discloses A circuit for reducing the current density on a bus (input bus lines of 26, 28) coupled to a plurality of circuits (26, 28), the circuit comprising: a first amplifier circuit (24A) of the plurality of circuits, wherein the first amplifier circuit has at least an output (output current of 24A) that is connected to the bus, and wherein the first amplifier circuit (24A) is configured to provide a first output current (output current of 24A) at the output of the first amplifier circuit; a first current source circuit (VCC/25E) having at least an output (common output node), wherein the output of the first current source circuit (VCC/25E) is connected to the bus (common output node), and wherein the first current source circuit (VCC/25E) is arranged to provide a first local current (current through 25E from potential difference between common node and VCC)) at an output of the first current source circuit (VCC/25E) such that at least a portion of the first output current (output current of 24A) is prevented from being carried on the bus (input bus lines of 26); and a second amplifier circuit (24C) of the plurality of circuits, wherein the second amplifier circuit has at least an output (output of 24C) that is connected to the bus , and wherein the second amplifier circuit (24C) is configured to provide a second output current (output current of 24C) at the output of the second amplifier circuit (24C).

Regarding claim 27, fig. 2 further comprising: a load circuit (26) that is connected to the bus; and a second current source circuit (VCC/25F) having at least an output (common node output), wherein the output of the second current source circuit is connected to the bus (input bus lines of 26), and wherein the second current source circuit I arranged to provide a second local current (current through 25F) at an output of

the second current source circuit such that at least a portion (24C) of the second output current is prevented (current of amplifier circuit is branched out at the common node input bus lines 26) from being carried on the bus.

Regarding claim 28, Fig. 2 of Galambos et al. discloses a circuit for reducing the current density, comprising: a first bus (top input bus line of 26), a second bus (bottom input bus line of 26), a third bus (top bus input bus line of 28), and a fourth bus (bottom input bus line of 28); a first amplifier circuit (24A) that is arranged to provide a first differential current (output current from left transistor of 24A), wherein the amplifier circuit (left transistor of differential amplifier 24A) is arranged to provide a first half of the first differential current (current output from left transistor of 24A) to the first bus (top input bus line of 26A), and to provide a second half of the first differential current (current output from right transistor of 24A) to the second bus (bottom bus line of 26), wherein the first amplifier circuit (24) has at least a first output that (output current of left transistor of 24A)is coupled to the first bus (top input bus line of 26) and a second output (output current from the right transistor of 24A) that is coupled to the second bus (bottom input bus line of 26); a second amplifier circuit (24C) that is arranged to provide a second differential current (output current 24C), wherein the amplifier circuit (24C) is arranged to provide a first half of the second differential current (output current from the right transistor of 24C) to the first bus (top input bus line of 26), and to provide a second half of the second differential current (output current from the left transistor of 24C) to the second bus (bottom input bus line of 26), wherein the second amplifier circuit (24) has at least a first output that is coupled to the first bus and a second output that is

coupled to the second bus (output currents from the left and right transistor of 24C are coupled to the top and bottom input bus lines of 26, respectively); a third amplifier circuit (24B) that is arranged to provide a third differential current (output current of 24C), wherein the amplifier circuit (24B) is arranged to provide a first half of the third differential current (output current from the left transistor of 24B) to the third bus (top input bus line of 28), and to provide a second half of the third differential current (output current from the right transistor of 24B) to the fourth bus (bottom input bus line of 28), wherein the third amplifier circuit (24B) has at least a first output that is coupled to the third bus and a second output that is coupled to the fourth bus (output currents from the left and right transistor of 24B are coupled to the top and bottom input bus lines of 28, respectively); a first current source circuit (VCC/25E) that is arranged to provide a first local current (current through 25E from potential between VCC and top input bus line of 26) at the first output of the first amplifier circuit (24A) such that at least a portion of the first half of the first differential current (output current from left transistor of 24A) is prevented from being carried on the first bus (top input bus line of 26); a second current source circuit (VCC/25F) that is arranged to provide a second local current (current through 25F from potential difference between VCC and bottom input bus line of 26) at the second output of the first amplifier circuit (24A) such that at least a portion of the second half of the first differential current (output current from the right transistor of 24A) is prevented from being carried on the second bus (bottom input bus line of 26); a third current source circuit (VCC/25C) that is arranged to provide a third local current (current through 25C from potential different between VCC and top input bus line 28) at the first

output of the third amplifier circuit (24B)such that at least a portion of the first half of the third differential current (output current from the left transistor of 24B) is prevented from being carried on the third bus (top input bus line of 28); and a fourth current source circuit (VCC/25D) that is arranged to provide a fourth local current (current through 25D from potential different between VCC and top input bus line 28) at the second output of (output current from the right transistor of 24B) the fourth amplifier circuit (output current from the right transistor of 24B) such that at least a portion of the second half of the third differential current (output current from the right transistor of 24B) is prevented from being carried on the fourth bus (bottom input bus line of 28).

Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Rexford Barnie can be reached at (571) 272-7492. The fax phone numbers for the organization where this application or proceeding is assigned are (571-273-8300) for regular communications and (571-273-8300) for After Final communications.

9/18/06

Linh Van Nguyen

Art Unit 2819

LINH NGUYEN
PRIMARY EXAMINER